REMARKS

Applicant concurrently files herewith a Petition (and fee) for a One-Month Extension of Time.

Claims 1-8 and 31-46 are all the claims presently being examined in this application. New Claims 43-46 have been added to more particularly define the invention. Claim 38 stands rejected upon informalities under 35 U.S.C. § 112, second paragraph.

Claims 1, 3-5, 7, 8, 34, 35, 37, 41 and 42 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Aoi (U.S. Patent No. 6,333,257 B1) in view of Jeng. (U.S. Patent No. 6,054,769). Claims 2, 6 and 31-33 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Aoi ('257) in view of Jeng ('769) and further in view of the applicant's admitted prior art. Claims 39 and 40 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Aoi ('257) in view of Jeng ('769) and further in view of Allada, et al. (U.S. Patent No. 6,218, 317 B1). Reconsideration is respectfully requested.

These rejections are respectfully traversed in view of the following discussion.

It is further noted that, notwithstanding any claim amendments made herein, Applicant's intent is to encompass equivalents of all claim elements, even if amended herein or later during prosecution.

It is noted that the amendments are made only to more particularly define the invention and not for distinguishing the invention over the prior art, for narrowing the scope of the claims, or for any reason related to a statutory requirement for patentability.

I. THE CLAIMED INVENTION

Applicant's invention, as disclosed and claimed, for example, by independent claim 1, and similarly independent claim 5, is directed to a semiconductor device having a multi-layered insulation film which includes a first insulation layer having an organic material with a dielectric constant which is lower than a silicon oxide dielectric constant, a second insulation layer including a polysiloxane compound having an Si-H group and formed on and adhering to a top of the first insulation layer, a third insulation layer comprising an inorganic material and formed on and adhering to a top of the second insulation layer, and a plurality of wires embedded in a groove formed in the multi-layered insulation film, the multi-layered insulation film being disposed between the wires. (See Page 13, lines 8-9; Page 20, lines 15-23; Page 21, lines 1-21; Page 22, last paragraph, last three-Page 23, line 9; and Figures 1-4).

Similarly, independent claim 42, recites in pertinent part, "the plurality of wires are embedded in a groove formed in the multi-layered insulation film."

Conventional devices have a first layer composed of an organic material of low dielectric, i.e., an organic SOG film e.g., Methyl Silsesquioxane ("MSQ") coated with a layer composed of an inorganic protective film, e.g., silicon oxide film, without a second insulation layer including a hydride organosiloxane. However, the conventional art is not effective because peeling occurs at the interface of the inorganic protective film and the organic layer, and thus de-lamination due to insufficient adhesion produces cross-talk in the semiconductor device . (See Page 2, lines 12-27; and Page 6, line 23 - Page 2, line 4).

An aspect of the invention includes a plurality of wires embedded in a groove formed in the multi-layered insulation film, the multi-layered insulation film being disposed between the wires, which reduces cross-talk between the wires and provides good interlayer adhesion,

which effectively prevents peering of the three insulation layers from each other. (See Page 12, line 25-Page 13, line 7; Page 16, lines 8-25; and Page 23, lines 10-15).

As a result of this inventive structure, process yield is improved and the semiconductor device is highly reliable as the interfacial adhesion between the film with low dielectric constant (e.g., the first insulation layer) and protective film, (e.g., the second insulation, adhesive layer), is significantly improved, "without damaging the excellent dielectric, flatness and gap-filling characteristics of the organic material of the low dielectric constant." (See Page 6, lines 15-20; and Page 13, lines 1-7).

II. THE 35 U.S.C. § 112, SECOND PARAGRAPH, REJECTION

In response to the rejection, Applicant has amended claim 38 to depend on claim 1 and further amended the claim to recite, "plurality of wires" in accordance with claim 1 and consistent with the specification. Accordingly, Applicant respectfully submits that the above amended claim 38 particularly points and distinctly claims the subject matter of the invention, and thus fulfills the requirements of 35 U.S.C. § 112, second paragraph.

In view of the foregoing, the Examiner is respectfully requested to withdraw this rejection.

III. THE PRIOR ART REJECTIONS

A. The 35 USC § 103(a) Rejection Based on Aoi in view of Jeng

First, the references, separately, or in combination, fail to teach, disclose or provide a reason or motivation for being combined. In particular, Aoi ("Aoi") pertains to an interconnection structure, and a related method, in a semiconductor integrated circuit. Aoi is

specifically directed to an inter-level insulating film with a low dielectric constant, with allegedly improved adherence to an organic film, an oxide film or a metal film, and thus increases adhesion between the metal interconnects and the first insulating film. (See Aoi at Abstract; Column 3, lines 1-835-45; and Column 6, lines 60-65).

By contrast, Jeng ("Jeng") does not have the same aim as Aoi.

Jeng discloses a structure, and a related method, which integrates polymer and other low dielectric constant materials into integrated circuit substrates. Jeng is specifically directed to reducing capacitance between closely spaced interconnect lines of integrated circuits. (See Jeng at Abstract; Column 1, lines 35-45; and Column 2, lines 38-53).

Nothing within Jeng, which focuses on improved adhesion between low dielectric constant materials and traditional inter-metal dielectric materials and protecting the low dielectric materials from subsequent processes," has anything to do with an inter-level insulating film with a low dielectric constant, with improved adherence to an organic film, an oxide film or a metal film as disclosed in Aoi. Thus, Aoi teaches away from being combined with another invention such as, for example, that of Jeng.

Therefore, one of ordinary skill in the art would not have combined these references, absent hindsight. It is clear that the Examiner has simply read Applicant's specification and conducted a keyword search to yield Aoi and Jeng. Further, the Examiner provides no motivation or reason to combine other than to assert that it would have been obvious to one having ordinary skill in the art at the time to combine these references. "to enable using a multi-layered dielectric film as taught by Jeng" to "reduce cross-talk between metal lines." Such an assertion does not take into account the distinct structural differences and related method of Aoi and Jeng as indicated above, and further discussed below. Thus, the

Examiner's assertion attempts to solve a problem which does not exist with either Aoi or Jeng, and this assertion is further proof of the Examiner's use of impermissible hindsight.

Second, even if combined, the references do not teach or suggest the features of independent claims 1, 5 and 42, (and similarly claim 41) including that a plurality of wires embedded in a groove formed in the multi-layered insulation film, the multi-layered insulation film being disposed between the wires. (See Page 13, lines 8-9; Page 20, lines 15-23; Page 21, lines 1-21; Page 22, last paragraph, last three-Page 23, line 9; and Figures 1-4).

Instead, Figures 1(a)-3(c) of Aoi merely disclose an interconnection structure in a semiconductor integrated circuit including an interlevel insulating film. The Office Action mischaracterizes Aoi because Aoi teaches a first metal interconnect 101, including a first silicon nitride film 102 formed over the first metal interconnect 101, a first organic-containing silicon dioxide film 103 formed on film 102, a second silicon nitride film 104 formed on film 103, and second organic-containing silicon dioxide film 105 formed over film 104. (See Office Action, Page 3, Section 6).

Further, contact holes 107 and wiring grooves 109 are formed in the four films 102-105 and a metal film 110 is deposited in the contact holes 107 and wiring grooves 109. "As a result, second metal interconnects 111 and contacts 112, interconnecting the first and second metal interconnects 101 and 11, are formed out of the metal film 110. (See Column 7, line 54-Column 8, line 65; and Figures 1(a)-3(c)). Accordingly, the wiring groove 109 is formed in a four layered structure including four layers 102, 103, 104 and 105.

In contrast, Applicant's invention includes a plurality of wires formed in a groove (e.g., respectively formed in a plurality of grooves) formed in a multi-layered insulation film, which includes three insulation layers, including a first insulation layer, a second insulation

layer and third insulation layer where the composition of the second insulation layer 3 comprises at least one of hydrogen silsesquioxane and a hydride organosiloxane not a silicon dioxide layer as in Aoi. Therefore, Aoi does not disclose, teach or suggest, including the features a plurality of wires embedded in a groove formed in the multi-layered insulation film, the multi-layered insulation film being disposed between the wires as recited in Applicant's invention.

In fact, the Examiner attempts to equate layers 18, 20 and 22 in Jeng with the multi-layered film of the invention. However, this interpretation is clearly incorrect. Indeed, in the present invention, the multi-layered film includes "a groove" in which a wire is embedded. (See Application, Figure 1). This feature is clearly not taught or suggested by Jeng.

Consequently, neither Aoi nor Jeng are capable of achieving at least one object of the invention, which includes improving process yield and increasing reliability of the semiconductor device. Accordingly, Applicant's invention provides for significantly improved interfacial adhesion between the film with low dielectric constant, i.e., the first insulation layer, and protective film, i.e., the second insulation, adhesive layer, "without damaging the excellent dielectric, flatness and gap-filling characteristics of the organic material of the low dielectric constant." (See Page 6, lines 15-20; and Page 13, lines 1-7). Thus, Applicant traverses the assertion that Aoi, alone, or in combination, teaches Applicant's invention, as recited above.

For at least the reasons outlined above, Applicant respectfully submits that Aoi in view of Jeng does not teach or suggest all the features of independent claims 1, 5, 41 and 42, and related dependent claims 3, 4, 7, 8, and 34-38.

Regarding the dependent claims 3, 4, 7, 8 and 34-38, which depend from claims 1 and

5, these claims are patentable not only by virtue of their dependency from their respective independent claims but also by the additional limitations they recite.

For the reasons stated above, the claimed invention is fully patentable over the cited references.

B. The § 103(a) Rejection Based on Aoi in view of Jeng and further in view of the Admitted Prior Art

Regarding claims 2, 6 and 31-33, to make up for the deficiencies of Aoi and Jeng, the Examiner relies on the Applicant's Admitted Prior Art ("APA"). The APA fails to do so.

First, the APA, pertains to a process of forming a damascene copper wiring system of a low dielectric constant material. APA is specifically directed to decreasing inter-wire capacity in order to cope with the higher-speed operation of semiconductor devices. (See Application, Background Section, Page 1, 2nd and 3rd Paragraphs, lines 8-15).

Nothing within APA, which focuses on decreasing the inter-wire capacity in order to cope with the higher-speed operation of semiconductor devices, has anything to with an interlevel insulating film with a low dielectric constant, with improved adherence to an organic film, an oxide film or a metal film as disclosed in Aoi. Further, nothing within APA, as indicated above, has anything to do with improved "adhesion between low dielectric constant materials and traditional intermetal dielectric materials and protecting the low dielectric materials from subsequent processes,"as disclosed in the Jeng. Thus, Aoi teaches away from being combined with another invention such as, for example, Jeng or APA.

Neither Jeng nor APA, separately, or in combination, has the same aim as Aoi as discussed above, and the urged combination would not have been made, absent hindsight.

Secondly, like Jeng and Aoi, the APA does not disclose, teach or suggest, a plurality of wires embedded in a groove formed in the multi-layered insulation film (e.g., a film having at least 3 layers), the multi-layered insulation film being disposed between the wires as recited in independent claims 1 and 5.

Instead, the APA merely discloses a curing system in which wires are formed in an insulation film having only two layers. The Application specifically explains the problems with such a design, and how the present invention having a multi-layered film (e.g., including at least three layers) overcomes these problems.

Thus, APA would not have been combined with Aoi and Jeng, and does not teach or suggest, including that a plurality of wires embedded in a groove formed in the multi-layered insulation film, the multi-layered insulation film being disposed between the wires.

For the reasons stated above, the claimed invention, and the invention as cited in independent claims 1 and 5, and related dependent claims 2, 6 and 31-33, should be fully patentable over the cited references.

C. The § 103(a) Rejection Based on Aoi in view of Jeng and further in view of Allada, et al.

Regarding claims 39 and 40, to make up for the deficiencies of Aoi and Jeng, the Examiner relies on Allada, et al. ("Allada"). Allada fails to do so.

First, Allada pertains to multilevel interconnects for integrated circuit devices, in particular, copper/dual damascene devices, and related fabrication methods. The interconnect integration eliminates "the need for removal of the wafer after formation of a polymeric interlayer dielectric to equipment for forming conventional oxide hardmasks on interlayer dielectrics." This invention is specifically directed to "increas[ing] device speed by reducing

the effective dielectric constant in the stack, and the structures created thereby." (See Allada at Abstract; Column 1, lines 7-12; and Column 2, lines 5-25).

Nothing within Allada, which focuses on increasing device speed by reducing the effective dielectric constant in the stack, and the structures created thereby, has anything to with an interlevel insulating film with a low dielectric constant, with improved adherence to an organic film, an oxide film or a metal film as disclosed in Aoi. Further, nothing within Allada, as indicated above, has anything to do with improved "adhesion between low dielectric constant materials and traditional intermetal dielectric materials and protecting the low dielectric materials from subsequent processes,"as disclosed in the Jeng. Thus, Aoi teaches away from being combined with another invention such as, for example, Jeng or Allada.

Neither Jeng nor Allada, separately, or in combination, has the same aim as Aoi as discussed above, and the urged combination would not have been made, absent hindsight.

Secondly, Allada does not disclose, teach or suggest, including that a plurality of wires embedded in a groove formed in the multi-layered insulation film, the multi-layered insulation film being disposed between the wires as recited in independent claim 1.

Further, Allada does not disclose, teach or suggest, including the second insulation film includes a methylated hydrogen silsesquioxane (MHSQ) film as recited in claim 39 of the invention. Allada also does not disclose, teach or suggest, including the MHSQ film has a thickness of about 50 nm as recited in claim 40 of the invention.

Instead, Figures 1a-1b of Allada teach multilevel interconnects for integrated circuit devices, in particular, copper/dual damascene devices, and related fabrication methods. "Methylated-oxide type hardmasks 18 are formed over polymeric interlayer dielectric

materials 16" where the hardmask and the interlayer dielectric may be spincoated. The "[d]ielectric layer 16 is etched and then electroplated with copper to produce the single damascene structure 10 with a copper line 20." Accordingly, a single metal copper line 20 is embedded in a recess formed between the methylated-oxide hardmask 18 and the interlayer dielectric material 16.

Clearly, Allada does not teach or suggest a plurality of wires embedded in a groove formed in the multi-layered insulation film, the multi-layered insulation film being disposed between the wires. Indeed, Allada is completely unrelated to the claimed invention.

Thus, Allada would not have been combined with Aoi and Jeng, and does not teach or suggest, including that a plurality of wires embedded in a groove formed in the multi-layered insulation film, the multi-layered insulation film being disposed between the wires.

For the reasons stated above, the claimed invention, and the invention as cited in independent claim 1, and related dependent claims 39 and 40, should be fully patentable over the cited references.

IV. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 1-8 and 31-46, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

Date: 12/1/03

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